We claim:

1. A pulse generation circuit for generating a pulse responsive to a trigger signal having a first and a second state, the pulse generation circuit comprising:

a passgate circuit having an input terminal adapted to receive the trigger signal, the passgate circuit having a passing state when enabled and a blocking state when disabled;

a gating circuit coupled to the passgate circuit, the gating circuit adapted to receive a first control signal derived from the trigger signal, the gating circuit configured to enable the passgate responsive to the control signal during a period at least encompassing the transition of the trigger signal from the first state to the second state; and

a reset circuit coupled to the gating circuit and coupled to the passgate circuit, the reset circuit adapted to disable the passgate responsive to the control signal at a time subsequent to the transition of the trigger signal from the first state to the second state.

2. The pulse generation circuit of claim 1, further comprising an amplification circuit configured to receive the pulse as an input and produce an Input/Output pull-up signal at an output terminal.

3. The pulse generation circuit of claim 2 wherein the amplification circuit comprises a first and a second inverter, serially coupled, the first inverter coupled to the passgate circuit and adapted to accept the pulse at an input and produce an inverted and amplified signal at an output, the second inverter adapted to accept the output of the first inverter at an input and produce the Input/Output pull-up signal at an output.

4. The pulse generation circuit of claim 1 wherein the trigger signal is a periodic signal.

5. The pulse generation circuit of claim 1 wherein the pulse generated is a positive pulse, the first state of the trigger signal is a LOW state, and the reset circuit couples the output terminal of the passgate circuit to a ground voltage when it disables the passgate.

6. The pulse generation circuit of claim 1 wherein the gating circuit further comprises:

an inverter having an input terminal to receive the trigger signal and producing an inverted signal;

a delay circuit coupled to the inverter, the delay circuit accepting the inverted signal at an input and passing it to an output after a pre-selected time delay; and

a logic gate having a plurality of inputs and an output, the logic gate adapted to accept at least the signal passed from the delay circuit, the logic gate generating a gating signal to enable the passgate.

7. The pulse generation circuit of claim 1 wherein the control signal is derived from the generated pulse.

8. A pull-up circuit to generate an Input/Output pull-up signal comprising:

a passgate circuit adapted to pass a periodic pulse received at an input terminal to an output terminal, responsive to an enable signal received at an enable terminal, and adapted to block the periodic pulse from being passed responsive to a disable signal received at the enable terminal;

control circuitry coupled to the passgate circuit and adapted to receive a control signal derived from the periodic pulse, the control circuitry generating the enable signal and the disable signal responsive to the control signal;

a bias circuit coupled to the control circuitry and the passgate, the bias circuit adapted to bias the output terminal to a first state responsive to the disable signal; and

a rectifyng circuit receiving the signal passed by the passgate circuit and converting it into the Input/Output pull-up signal.

9. The pull-up circuit of claim 8 wherein the rectifying circuit comprises a first and a second inverter, serially coupled, the first inverter coupled to the passgate circuit and adapted to accept the signal passed by the passgate circuit at an input and produce an inverted and amplified signal at an output, the second inverter adapted to accept the output of a first inverter at an input and produce the Input/Output pull-up signal at an output.

10. The pull-up circuit of claim 8 wherein the periodic pulse is a clock signal.

11. The pull-up circuit of claim 8 wherein the pulsed passed by the passgate circuit is a positive pulse, the beginning of which is generated when the periodic pulse changes from a first to a second state, and the end of which is generated when the bias circuit operates on the output terminal.

12. The pull-up circuit of claim 8 wherein the enable signal is generated before the passgate receives the periodic signal to pass to the output terminal.

13. The pull-up circuit of claim 8 wherein the control signal is derived from the pulse passed by the passgate.

14. A one-shot circuit for generating a pulse using a trigger signal as an input, the one-shot circuit comprising:

an input terminal adapted to accept a trigger signal having a first state and a second state;

a generated pulse output terminal coupled to the input terminal;

a control circuit coupled to the input and generated pulse output terminals, the control circuit having at least one control input accepting a control signal, the control signal decoded by the control circuit to pass or block the trigger signal from the input terminal to the generated pulse output terminal; and

a reset switch coupled between the generated pulse output terminal and a reference voltage, the control circuit controlling the switch to connect the output terminal to a ground voltage responsive to the control signal.

15. The one-shot circuit of claim 14, further comprising an amplification circuit configured to receive the pulse as an input and produce an Input/Output pull-up signal at an output terminal.

16. The one-shot circuit of claim 15 wherein the amplification circuit comprises a first and a second inverter, serially coupled, the first inverter coupled to the generated pulse output terminal and accepting the generated pulse it an input, and producing an inverted and amplified signal at an output, the second inverter to accept the output of the first inverter at an input and produce the Input/Outpul pull-up signal at an output.

17. The one-shot circuit of claim 14 wherein the trigger signal is enabled to pass from the input terminal to the output terminal before a transition from the first state to the second state of the trigger signal.

18. The one-shot circuit of claim 14 wherein the control signal is derived from the generated pulse.

19. The one-shot circuit of claim 14 wherein the trigger signal is one of the control signals received at one of the control inputs of the control circuit.

20. The one-shot circuit of claim 14 wherein the generated pulse is a positive pulse, the first state of the trigger signal is a LOW state, and wherein the reset switch couples the output terminal to a ground voltage responsive to the control signal.

21. The one-shot circuit of claim 14 wherein the control circuit further comprises:

an inverter which accepts the trigger signal and produces an inverted signal;

a delay circuit coupled to the inverter, the delay circuit accepting the inverted signal at an input and passing it to an output after a pre-selected delay; and

a logic gate having a plurality of inputs and an output, the logic gate adapted to accept the inverted signal passed from the delay circuit, the logic gate output coupled to a control input of the passgate.

22. A column decoder comprising:

digit lines coupled to Input/Output lines;

an address decoder adapted to decode an address received from an address bus and switchably couple selected digit lines to respective Input/Output lines;

an inactivation circuit adapted to switchably disconnect Input/Output lines from a bias voltage for a period following a transition of a periodic signal; and

an Input/Output biasing circuit including:

a passgate circuit having an input terminal adapted to receive the periodic signal, the passgate circuit having a passing state when enabled and a blocking state when disabled,

a gating circuit coupled to the passgate circuit, the gating circuit adapted to receive a first control signal derived from the periodic signal, the gating circuit configured to enable the passgate responsive to the control signal during a period at least encompassing the transition of the periodic signal from a first state to a second state, and

a reset circuit coupled to the gating circuit and coupled to the passgate circuit, the reset circuit adapted to disable the passgate responsive to the control signal at a time subsequent to the transition of the periodic signal from the first state to the second state.

23. The column decoder of claim 22 wherein the periodic signal is a clock signal.

24. The column decoder of claim 22 wherein a pulse generated by the passgate is a positive pulse, the first edge of the periodic signal is a rising edge, and the reset circuit couples the output terminal of the passgate circuit to a ground voltage when it disables the passgate.

25. The column decoder of claim 22 wherein the control signal is derived from a generated pulse.

26. A clock buffer circuit for transferring a clock signal from an input terminal to an output terminal comprising:

a passgate circuit adapted to receive a clock signal having a first state and a second state, the passgate blocking or passing the clock signal responsive to an enable signal;

an enable generating circuit coupled to the passgate circuit, the enabled generating circuit adapted to decode a control signal derived from the clock signal and received at an input terminal, and adapted to generate an enable signal during a period at least during a transition of the clock signal from the first state to the second state; and

a disable circuit coupled to the enable generating circuit and the passgate circuit, the disable circuit adapted to return the output of the passgate circuit to a first state at a time subsequent to the enable signal being generated.

27. The clock buffer circuit of claim 26 wherein the enable signal is generated prior to a rising edge of the clock signal and the disable circuit couples the output of the passgate circuit to a ground voltage.

28. The clock buffer circuit of claim 26 wherein the control signal is derived from the output of the passgate circuit.

29. A synchronous memory device comprising:

an address bus;

a control bus;

a data bus;

a clock terminal adapted to receive a clock signal;

a clock enable terminal adapted to receive a clock enable signal;

an address decoder coupled to the address bus;

a control logic circuit coupled to the control bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, including

a plurality of row lines;

a plurality of pairs of first and second complementary digit lines;

an array of memory cells that each have a control terminal coupled to one of the row lines and a data terminal coupled to one of the first and second complementary digit lines of one of the pairs of complementary column lines; and

a pulse generation circuit for generating a pulse responsive to a trigger signal having a first and a second state, the pulse generation circuit including:

a passgate circuit having an input terminal adapted to receive the trigger signal, the passgate circuit having a passing state when enabled and a blocking state when disabled,

a gating circuit coupled to the passgate circuit, the gating circuit adapted to receive a first control signal derived from the trigger signal, the gating circuit configured to enable the passgate responsive to the control signal during a period at least encompassing the transition of the trigger signal from the first state to the second state, and

a reset circuit coupled to the gating circuit and coupled to the passgate circuit, the reset circuit adapted to disable the passgate responsive to the control signal at a time subsequent to the transition of the trigger signal from the first state to the second state.

30. The pulse generation circuit of claim 29, further comprising an amplification circuit configured to receive the pulse as an input and produce an Input/Output pull-up signal at an output terminal.

31. The pulse generation circuit of claim 30 wherein the amplification circuit comprises a first and a second inverter, serially coupled, the first inverter coupled to the passgate circuit and adapted to accept the pulse signal at an input and produce an inverted and amplified signal at an output, the second inverter adapted to accept the output of the first inverter at an input and produce the Input/Output pull-up signal at an output.

32. The pulse generation circuit of claim 29 wherein the trigger signal is a periodic signal.

33. The pulse generation circuit of claim 32 wherein the periodic signal is a clock signal.

34. The pulse generation circuit of claim 29 wherein the pulse generated is a positive pulse, the first state of the trigger signal is a LOW state, and the reset circuit couples the output terminal of the passgate circuit to a ground voltage when it disables the passgate.

35. The pulse generation circuit of claim 29 wherein the gating circuit further comprises:

an inverter having an input terminal to receive the trigger signal and producing an inverted signal;

a delay circuit coupled to the inverter, the delay circuit accepting the inverted signal at an input and passing it to an output after a preselected time delay; and

a logic gate having a plurality of inputs and an output, the logic gate adapted to accept at least the signal passed from the delay circuit, the logic gate generating a gating signal to enable the passgate.

36. A computer system comprising:

a data input device;

a data output device;

an address bus;

a data bus;

a control bus; and

computing circuitry coupled to the data input and output devices, and the data, address and control busses, the computing circuitry including:

a pulse generation circuit for generating a pulse responsive to a trigger signal having a first and a second state, the pulse generation circuit comprising:

a passgate circuit having an input terminal adapted to receive the trigger signal, the passgate circuit having a passing state when enabled and a blocking state when disabled,

a gating circuit coupled to the passgate circuit, the gating circuit adapted to receive a first control signal derived from the trigger signal, the gating circuit configured to enable the passgate responsive to the control signal during a period at least encompassing the transition of the trigger signal from the first state to the second state, and

a reset circuit coupled to the gating circuit and coupled to the passgate circuit, the reset circuit adapted to disable the passgate responsive to the control signal at a time subsequent to the transition of the trigger signal from the first state to the second state.

37. The pulse generation circuit of claim 36, further comprising an amplification circuit configured to receive the pulse as an input and produce an Input/Output pull-up signal at an output terminal.

38. The pulse generation circuit of claim 37 wherein the amplification circuit comprises a first and a second inverter, serially coupled, the first inverter coupled to the passgate circuit and adapted to accept the pulse signal at an input and produce an inverted and amplified signal at an output, the second inverter adapted to accept the output of the first inverter at an input and produce the Input/Output pull-up signal at an output.

39. The pulse generation circuit of claim 36 wherein the trigger signal is a periodic signal.

40. The pulse generation circuit of claim 39 wherein the periodic signal is a clock signal.

41. The pulse generation circuit of claim 36 wherein the pulse generated is a positive pulse, the first edge of the trigger signal is a rising edge, and the reset circuit couples the output terminal of the passgate circuit to a ground voltage when it disables the passgate.

42. The pulse generation circuit of claim 36 wherein the gating circuit further comprises:

an inverter having an input terminal to receive the trigger signal and producing an inverted signal;

a delay circuit coupled to the inverter, the delay circuit accepting the inverted signal at an input and passing it to an output after a preselected time delay; and

a logic gate having a plurality of inputs and an output, the logic gate adapted to accept at least the signal passed from the delay circuit, the logic gate generating a gating signal to enable the passgate.

43. A method for generating a pulse responsive to a trigger signal transitioning from a first state to a second state, the method including the steps of:

applying a trigger signal to a passgate;

enabling the passgate for a period of time at least encompassing the transition of the trigger signal from a first state to a second state; and

disabling the passgate at a predetermined time subsequent to the transition of the trigger signal.

44. The method for generating a pulse of claim 43, further including the step of:

biasing an output of the passgate to a first state when the passgate is disabled.

45. The method for generating a pulse of claim 43 wherein the step of enabling the passgate depends from the trigger signal.

46. The method for generating a pulse of claim 43 wherein the step of enabling the passgate depends from an output of the passgate.

47. The method for generating a pulse of claim 43 wherein the trigger signal is a periodic signal.

48. A method of generating a pulse in a synchronous memory, the method comprising the steps of:

applying a trigger signal to a passgate;

enabling the passgate for a period of time at least encompassing the transition of the trigger signal from a first state to a second state; and

disabling the passgate at a predetermined time subsequent to the transition of the trigger signal.

49. The method for generating a pulse of claim 48, further including the step of:

biasing an output of the passgate to a first state when the passgate is disabled.

50. The method for generating a pulse of claim 48 wherein the step of enabling the passgate depends from the trigger signal.

51. The method for generating a pulse of claim 48 wherein the step of enabling the passgate depends from an output of the passgate.

52. The method for generating a pulse of claim 48 wherein the trigger signal is a periodic signal.

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